Amendments of the Claims:

A detailed listing of all claims in the application is presented below. This listing of claims will replace all prior versions, and listings, of claims in the application. All claims being currently amended are submitted with markings to indicate the changes that have been made relative to immediate prior version of the claims. The currently amended are Claims 5 and 11. Claims 13 - 20 are new. Claims 1 - 4, 6 - 10, and 12 are canceled. The changes in any amended claims are being shown by strikethrough (for deleted matter) or underlined (for added matter).

1. (Canceled) A method for efficient access to multiple lines of image data using a memory device with at least one memory module, wherein each memory module has at least one bank with multiple rows, the method comprising the steps of:
maintaining address information of a current row for each bank within each memory module;
receiving a request for an incoming row; and
determining if the incoming row matches the current row based on the address information and if so, immediately accessing the current row without closing and reopening the current row.

2. (Canceled) The method according to Claim 1 wherein the step of maintaining address information comprises the steps of:
setting an open bit when the current row is opened; and clearing the open bit when the current row is closed.

3. (Canceled) The method according to Claim 1 further comprising the step of maintaining programmable counters to monitor timing parameters and detect legal and illegal actions.

4. (Canceled) The method according to Claim 1 further comprising the step of positioning adjacent lines of the image data in separate memory banks to optimize access to multiple lines of the image data.

5. (Currently amended) ~~The method according to Claim 1 further comprising the step of:~~
A method for efficient access to multiple lines of image data using a memory device with at least one memory module, wherein each memory module has at least one bank with multiple rows, the method comprising the steps of:
maintaining address information of a current row for each bank within each memory module;
receiving a request for an incoming row;
determining if the incoming row matches the current row based on the address information and if so, immediately accessing the current row without closing and reopening the current row;
receiving a request for a desired memory format from an external structure; and
selecting the desired memory format from different address multiplexing schemes.

6. (Canceled) The method according to Claim 1 wherein the memory modules are SDRAM modules, each having four banks.

7. (Canceled) A memory controller for efficient access to multiple lines of image data using at least one memory module, wherein each memory module has at least one bank with multiple rows, the memory controller comprising:
means for maintaining address information of a current row for each bank within each memory module;
means for receiving a request for an incoming row; and means for determining if the incoming row matches the current row based on the address information and if so, immediately accessing the current row without closing and reopening the current row.

8. (Canceled) The memory controller according to Claim 7 wherein the means for maintaining address information comprises:
means for setting an open bit when the current row is opened; and
means for clearing the open bit when the current row is closed.

9. (Canceled) The memory controller according to Claim 7 further comprising programmable counters maintained to monitor timing parameters and detect legal and illegal actions.

10. (Canceled) The memory controller according to Claim 7 wherein adjacent lines of the image data are positioned in separate memory banks to optimize access to multiple lines of the image data.

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11. (Currently amended) ~~The memory controller according to Claim 7 further comprising:~~

A memory controller for efficient access to multiple lines of image data using at least one memory module, wherein each memory module has at least one bank with multiple rows, the memory controller comprising:

means for maintaining address information of a current row for each bank within each memory module;

means for receiving a request for an incoming row; and means for determining if the incoming row matches the current row based on the address information and if so, immediately accessing the current row without closing and reopening the current row;

means for receiving a request for a desired memory format from an external structure; and

means for selecting the desired memory format from different address multiplexing schemes.

12. (Canceled) The memory controller according to Claim 7 wherein the memory modules are SDRAM modules, each having four banks.

13. (New) The method according to Claim 5 wherein the step of maintaining address information comprises the steps of:

setting an open bit when the current row is opened; and clearing the open bit when the current row is closed.

14. (New) The method according to Claim 5 further comprising the step of maintaining programmable counters to monitor timing parameters and detect legal and illegal actions.

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15. (New) The method according to Claim 5 further comprising the step of positioning adjacent lines of the image data in separate memory banks to optimize access to multiple lines of the image data.

16. (New) The method according to Claim 5 wherein the memory modules are SDRAM modules, each having four banks.

17. (New) The memory controller according to Claim 11 wherein the means for maintaining address information comprises:
means for setting an open bit when the current row is opened; and
means for clearing the open bit when the current row is closed.

18. (New) The memory controller according to Claim 11 further comprising programmable counters maintained to monitor timing parameters and detect legal and illegal actions.

19. (New) The memory controller according to Claim 11 wherein adjacent lines of the image data are positioned in separate memory banks to optimize access to multiple lines of the image data.

20. (New) The memory controller according to Claim 11 wherein the memory modules are SDRAM modules, each having four banks.